



STL11N4LLF5

N-channel 40 V, 9.1 mΩ typ., 15 A STripFET™V Power MOSFET
in a PowerFLAT™ 3.3 x 3.3 package

Datasheet – production data

Features

Order code	V _{DS}	R _{DS(on)} max	I _D
STL11N4LLF5	40 V	9.7 mΩ	15 A

- Low gate charge
- Very low on-resistance
- High avalanche ruggedness

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using STMicroelectronics' STripFET™V technology. The device has been optimized to achieve very low on-state resistance, contributing to a FOM that is among the best in its class.

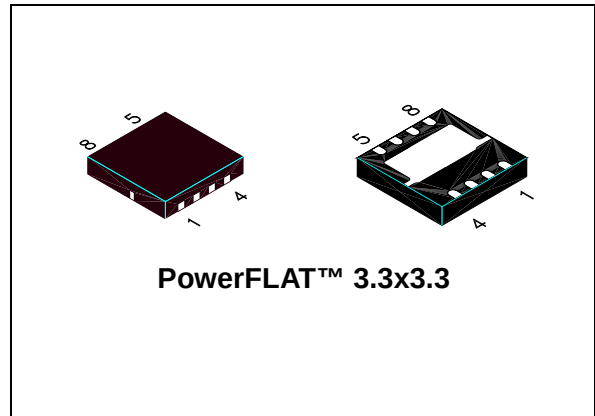


Figure 1. Internal schematic diagram

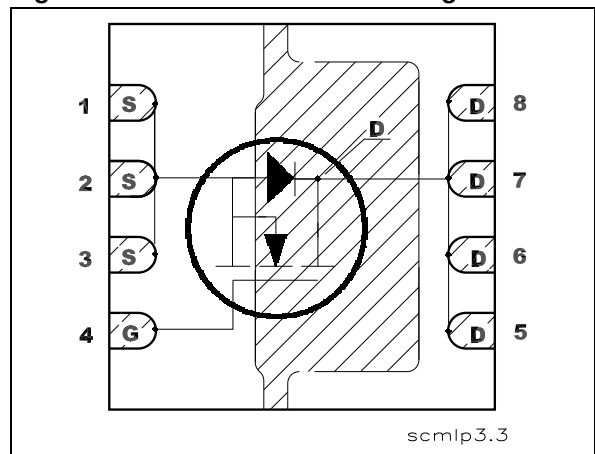


Table 1. Device summary

Order code	Marking	Package	Packaging
STL11N4LLF5	11N4LLF5	PowerFLAT™ 3.3 x 3.3	Tape and reel

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	40	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_{pcb} = 25\text{ }^{\circ}\text{C}$	11	A
$I_D^{(1)}$	Drain current (continuous) at $T_{pcb}=100\text{ }^{\circ}\text{C}$	6.8	A
$I_{DM}^{(2)}$	Drain current (pulsed)	44	A
$P_{TOT}^{(3)}$	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	50	W
$P_{TOT}^{(1)}$	Total dissipation at $T_{pcb} = 25\text{ }^{\circ}\text{C}$	2.9	W
	Derating factor ⁽³⁾	0.4	W/ $^{\circ}\text{C}$
T_J T_{stg}	Operating junction temperature storage temperature	-55 to 150	$^{\circ}\text{C}$

1. The value is rated according $R_{thj-pcb}$
2. Pulse width limited by safe operating area.
3. The value is rated according R_{thj-c}

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	2.5	$^{\circ}\text{C/W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	42.8	$^{\circ}\text{C/W}$
$R_{thj-pcb}^{(2)}$	Thermal resistance junction-pcb	63.5	$^{\circ}\text{C/W}$

1. When mounted on FR-4 board of 1inch² , 2oz Cu, $t < 10\text{sec}$
2. Steady state

2 Electrical characteristics

($T_{CASE}=25^{\circ}\text{C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0$	40			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 40\ \text{V}$, $V_{DS} = 40\ \text{V}$, $T_C = 125^{\circ}\text{C}$			1 10	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\ \text{V}$			± 100	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	1		2.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\ \text{V}$, $I_D = 5.5\ \text{A}$ $V_{GS} = 4.5\ \text{V}$, $I_D = 5.5\ \text{A}$		9.1 10.6	9.7 12	$\text{m}\Omega$ $\text{m}\Omega$

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\ \text{V}$, $f = 1\ \text{MHz}$, $V_{GS} = 0$		1570		pF
C_{oss}	Output capacitance			257		pF
C_{rss}	Reverse transfer capacitance			32		pF
Q_g	Total gate charge	$V_{DD} = 15\ \text{V}$, $I_D = 11\ \text{A}$		12.9		nC
Q_{gs}	Gate-source charge	$V_{GS} = 4.5\ \text{V}$		3.9		nC
Q_{gd}	Gate-drain charge	(see Figure 14)		5.3		nC
R_G	Gate input resistance	$f = 1\ \text{MHz}$ Gate DC Bias = 0 Test signal level = 20 mV $I_D = 0$	0.5	1.5	2.5	Ω

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 15\ \text{V}$, $I_D = 5.5\ \text{A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 4.5\ \text{V}$ (see Figure 13)	-	14	-	ns
t_r	Rise time			42		ns
$t_{d(off)}$	Turn-off delay time			37		ns
t_f	Fall time			5.2		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		11	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		44	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=11\text{ A}$, $V_{GS}=0$	-		1.1	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD}=11\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD}=20\text{ V}$, $T_j=150\text{ }^\circ\text{C}$ (see Figure 18)	-	27.2 24.5 1.8		ns nC A

1. Pulse width limited by safe operating area.

2. Pulsed: pulse duration=300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

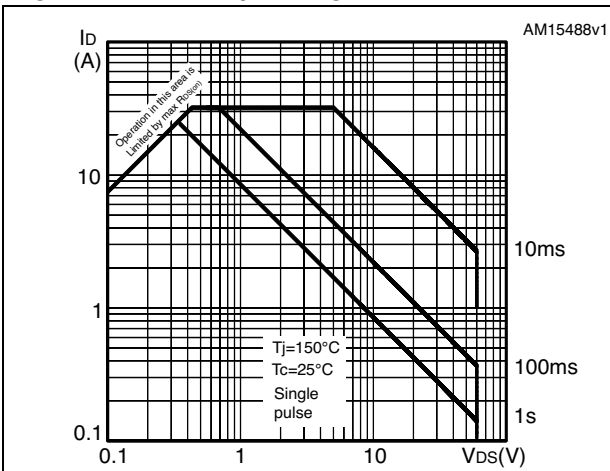


Figure 3. Thermal impedance

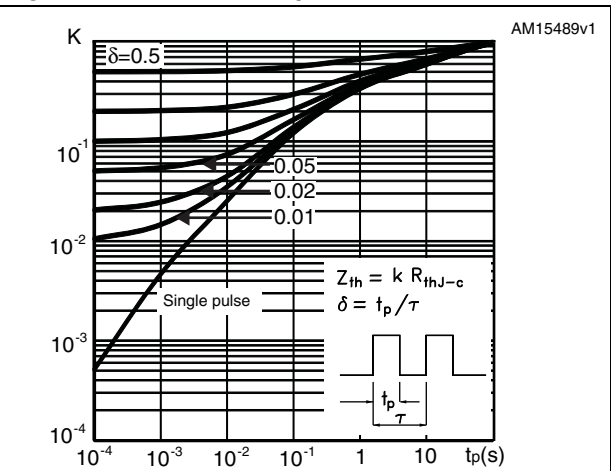


Figure 4. Output characteristics

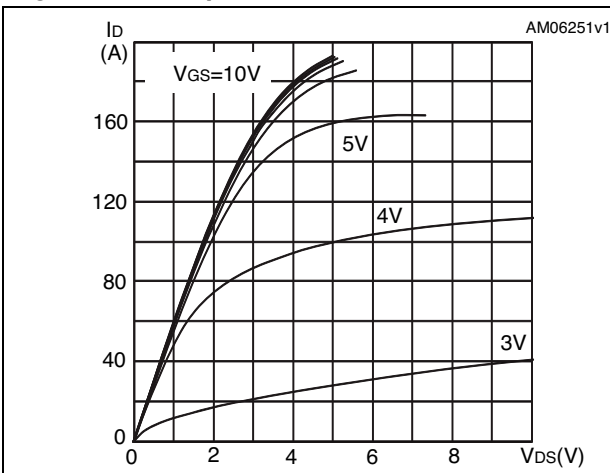


Figure 5. Transfer characteristics

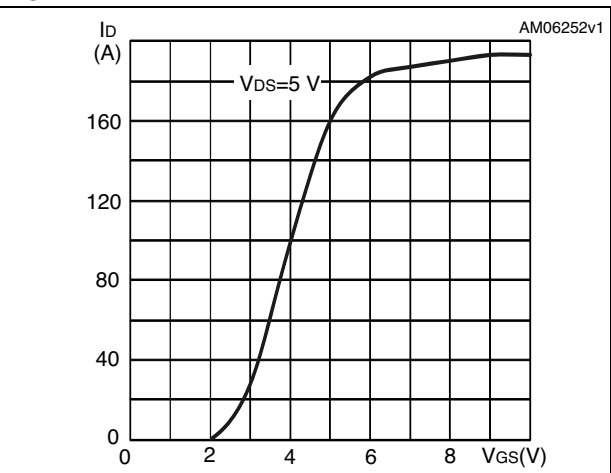


Figure 6. Normalized BVDS vs temperature

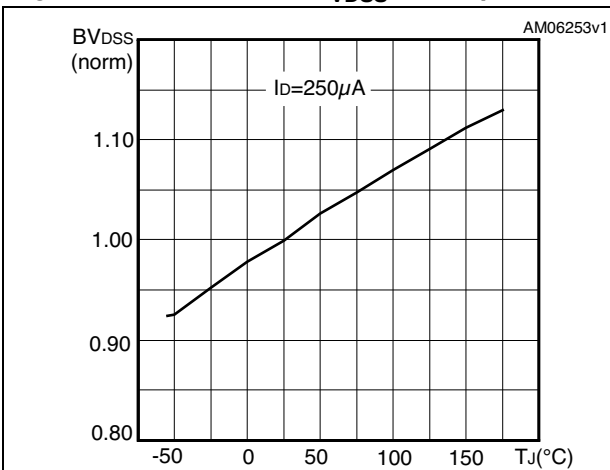


Figure 7. Static drain-source on-resistance

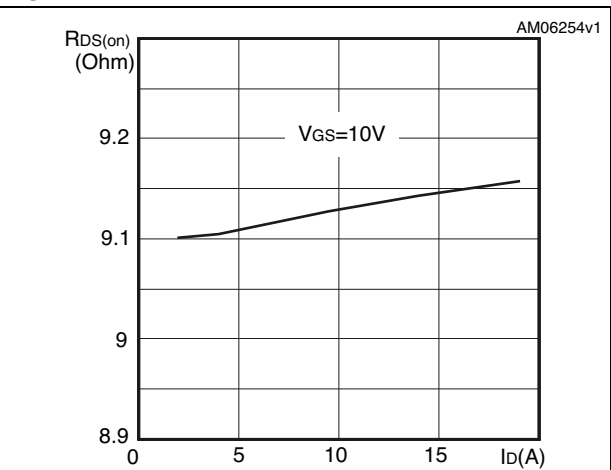


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

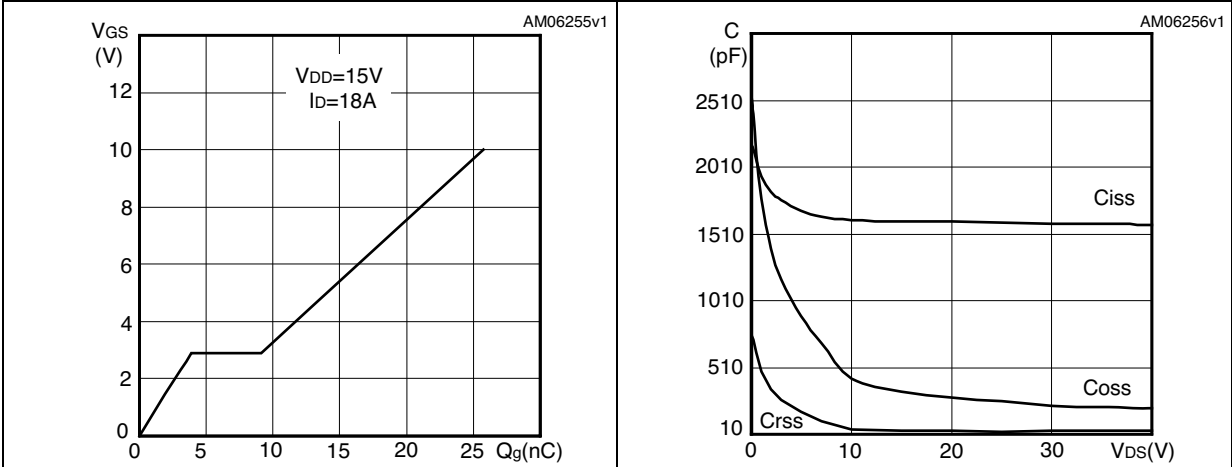


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on-resistance vs temperature

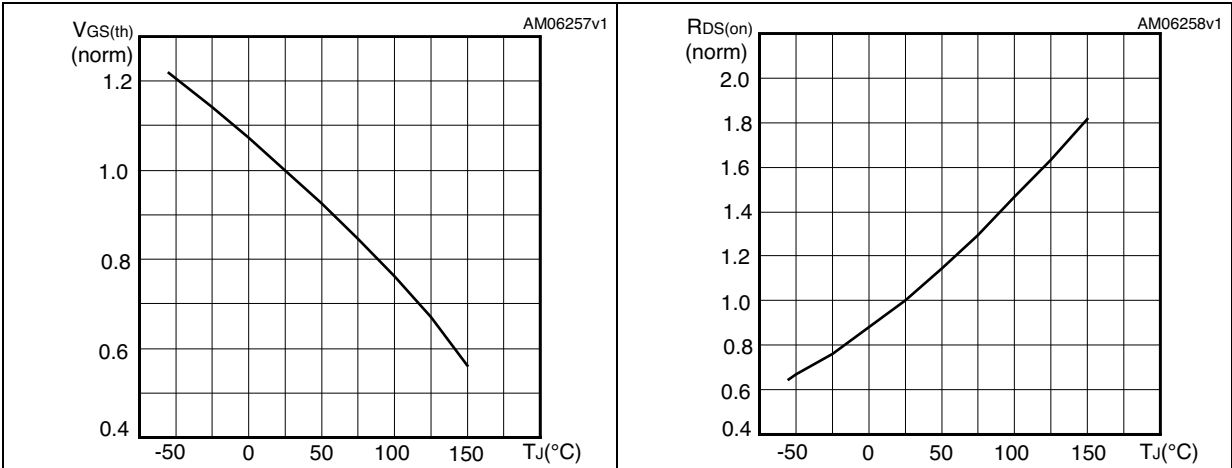
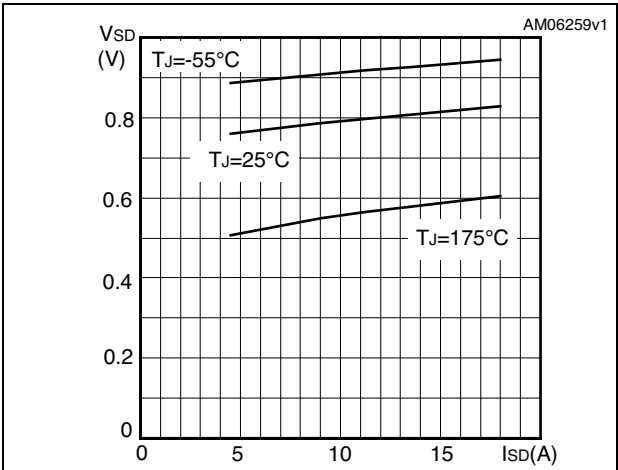


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

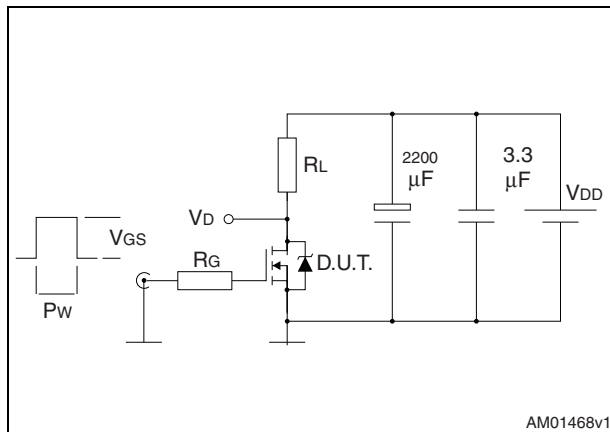


Figure 14. Gate charge test circuit

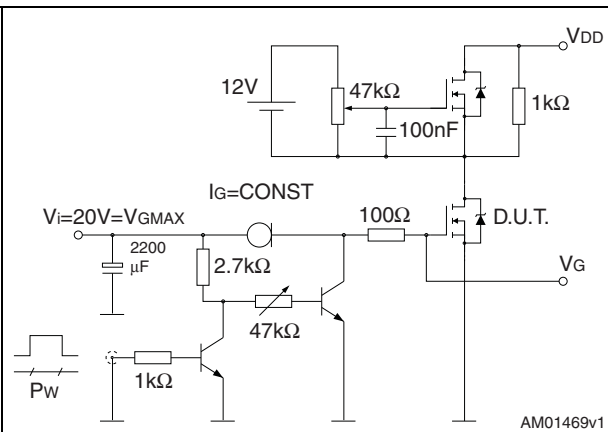


Figure 15. Test circuit for inductive load switching and diode recovery times

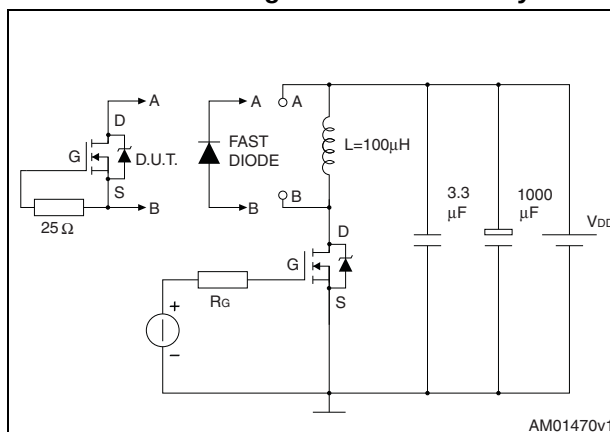


Figure 16. Unclamped inductive load test circuit

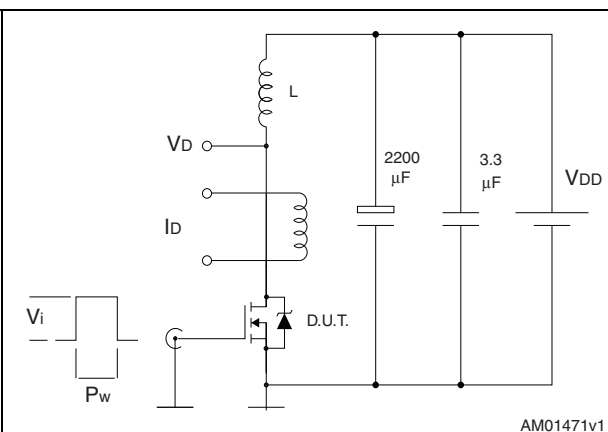


Figure 17. Unclamped inductive waveform

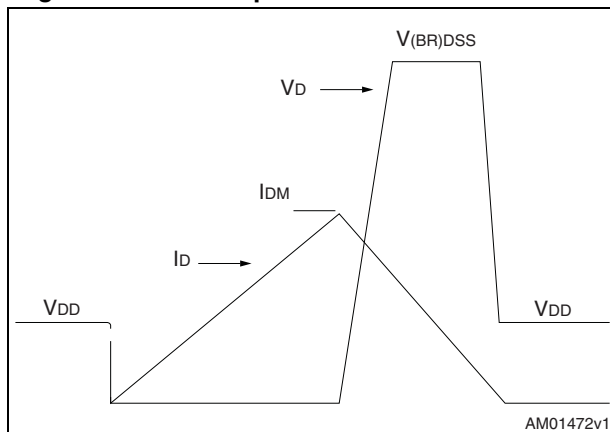
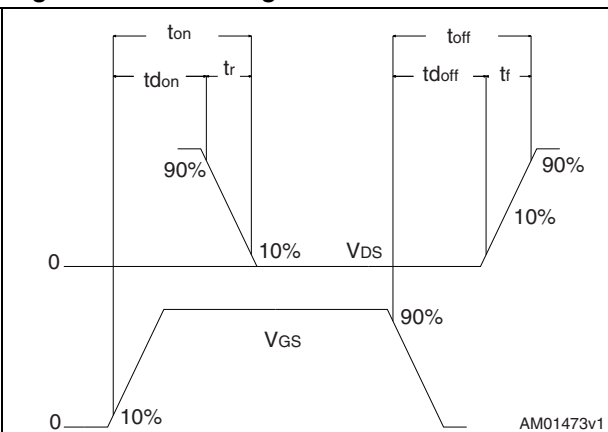


Figure 18. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Table 8. PowerFLAT™ 3.3 x 3.3 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0		0.05
A3		0.20	
b	0.23		0.38
D	3.20	3.30	3.40
D2	2.50		2.75
E	3.20	3.30	3.40
E2	1.25		1.50
e		0.65	
L	0.30		0.50

Figure 19. PowerFLAT™ 3.3 x 3.3 drawing

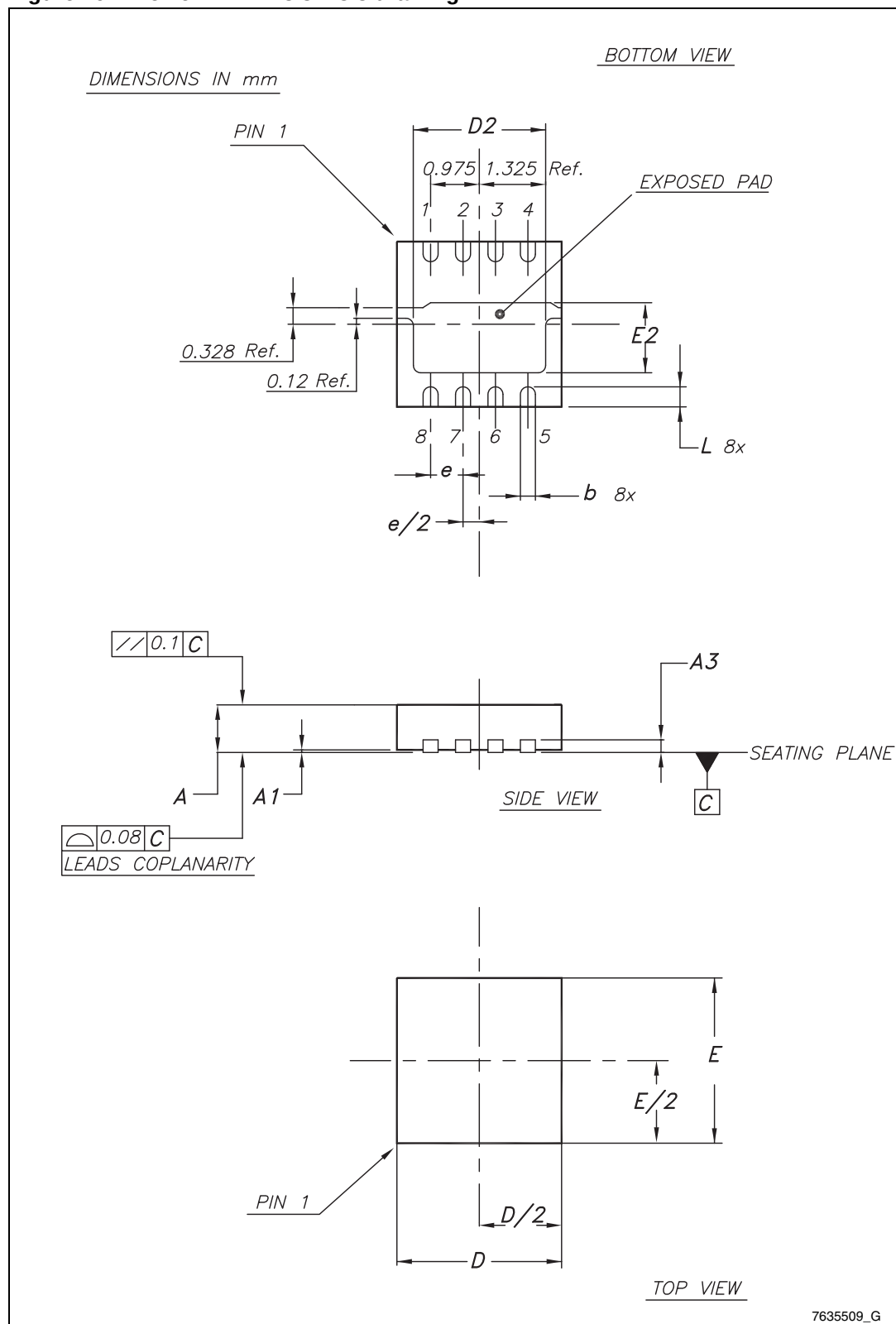
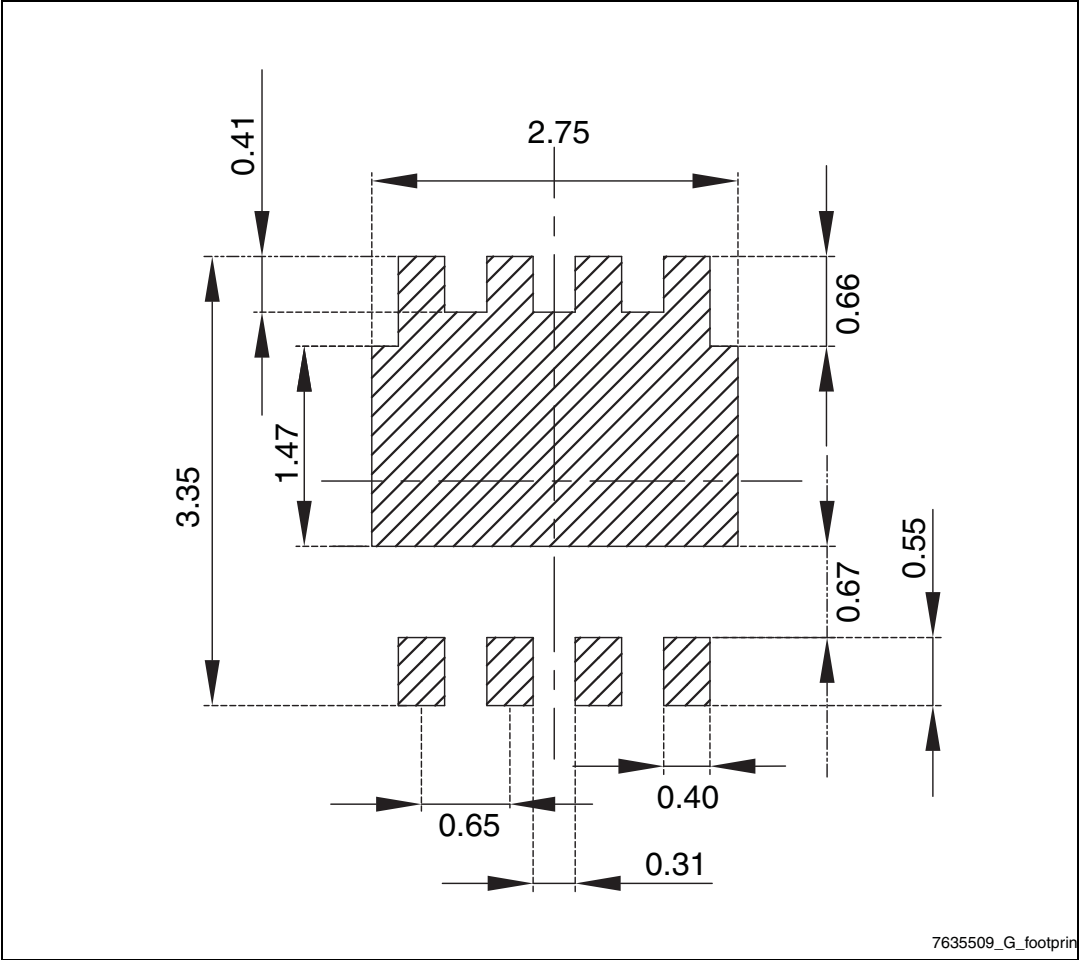


Figure 20. PowerFLAT™ 3.3 x 3.3 recommended footprint



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
19-Feb-2013	1	First release

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